Claims

1. A microprocessor, comprising:

a first register file containing registers;

a second register file containing registers; and

a facility for granting access to the first and second register files in a single thread mode and in a multi-thread mode, wherein, in the single thread mode, a single thread has access to both the first register file and the second register file and wherein, in the multi-thread mode, a first thread has access to the first register file and a second thread has access to the second register file.

2. The microprocessor of claim 1, wherein, in the single thread mode, the single thread has exclusive access to both the first register file and the second register file, relative to other threads.

3. The microprocessor of claim 1, wherein the facility includes a mechanism for switching between the single thread mode and the multi-thread mode.

4. The microprocessor of claim 3, wherein the mechanism includes control registers that control whether the microprocessor executes in the single thread mode or in the multi-thread mode.

5. The microprocessor of claim 4, wherein the mechanism includes software that writes appropriate values into the control registers to switch between the single thread mode and the multi-thread mode.

6. The microprocessor of claim 1, wherein the facility is a register renamer that maps logical register references in instructions to registers in the first register file and the second register file.

7. The microprocessor of claim 1, further comprising write lines extending between the first register file and the second register file so that contents of one of the first and second register files may be copied to the other of the first and second register files.

8. The microprocessor of claim 1, wherein the microprocessor supports simultaneous multi-threading.

9. In a microprocessor having a first register file and a second register file, a mapping mechanism for mapping references to registers in both the first register file and the second register file when in a single thread mode and for mapping references to registers in instructions of a first thread solely to registers in the first register file and references to registers in instructions in a second thread to registers in the second register file when in a multi-thread mode.

10. The mapping mechanism of claim 9, wherein the mapping mechanism switches between the single thread mode and the multi-thread mode when directed by a control mechanism.

11. In a microprocessor having multiple register sets, a method, comprising the steps of:

providing respective threads that are simultaneously executing in a multi-thread mode with access to separate respective ones of the register sets; and

switching from the multi-thread mode to a single thread mode where a single thread is executing and where the single thread has access to all the register sets.

12. The method of claim 11, wherein each of the register sets is a respective register file.

13. The method of claim 11, where two simultaneously executing threads are provided in the multi-thread mode.

14. The method of claim 11, wherein the microprocessor includes control registers and wherein the method further comprises prompting the switching by writing values in the control registers.

15. The method of claim 11, wherein the switching comprises propagating values held in a first of the register sets to a second of the register sets to regain coherence between the first and second register sets.

16. A microprocessor, comprising:

a first bank of execution units for executing instructions;

a second bank of execution units for executing instructions;

a first register file having read and write ports associated with the first bank of execution units and read and write ports associated with the second bank of execution units;

a second register file having read and write ports associated with the first bank of execution units and read and write ports associated with the second bank of execution units; and

circuitry for enabling or disabling selected ones of the read ports and the write ports to control access by threads to the register files.

17. The microprocessor of claim 16, wherein, in a single thread mode, the circuitry enables the read and write ports for both the first register file and the second register file for access by a single thread.

18. The microprocessor of claim 16, wherein, in a multi-thread mode, the circuitry enables the read and write ports associated with the first bank of execution units for the first register file for access by a first thread and disables the read and write ports associated with the second bank of execution units for the first register file so as to not be accessible by the first thread.

19. The microprocessor of claim 18, wherein, in the multi-thread mode, the circuitry enables the read and write ports associated with the second bank of execution units for the second register file for access by a second thread and disables the read and write ports associated with the first bank of execution units for the first register file so as to not be accessible by the second thread.

20. The microprocessor of claim 16 further comprising a register renamer for renaming logical references to registers in instructions so as to operate in one of a single thread mode or multi-thread mode of operation.